**Q103-002 Certification of Design and Construction**

Supplier Name:       Date:

The following information is required to identify a device that has met the requirements of AEC-Q103-002. Submission of the required data in the format shown below is optional. **All entries must be completed; if a particular item does not apply, enter "Not Applicable".** This template can be downloaded from the AEC website at http://www.aecouncil.com.

**This template is available as a stand-alone document.**

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| **Item Name** | **Supplier Response** | | | |
| 1. User’s Part Number: |  | | | |
| 2. Supplier’s Part Number/Data Sheet: |  | | | |
| 3. Device Description: |  | | | |
| 4.1. Control Wafer/Die Fab Location & Process ID:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 4.2. MEMS Wafer/Die Fab Location & Process ID:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 4.3. Cap Wafer/Die Fab Location & Process ID:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 4.4. Cap Wafer to MEMS Wafer Bonding Location & Process ID:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 5.1. Control Wafer Probe Location:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 5.2. MEMS Wafer Probe Location:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 5.3. Bonded Wafer Probe Location:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 6. Assembly Location & Process ID:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 7. Final Quality Control A (Test) Location:  a. Facility name/plant #:  b. Street address:  c. Country: |  | | | |
| 8.1. Control Wafer/Die:  a. Wafer size:  b. Die family:  c. Die mask set revision & name:  d. Die photo: | See attached  Not available | | | |
| 8.2. MEMS Wafer/Die:  a. Wafer size:  b. Die family:  c. Die mask set revision & name:  d. Die photo: | See attached  Not available | | | |
| 9.1. Control Wafer/Die Technology Description:  a. Wafer/Die process technology:  b. Die channel length:  c. Die gate length:  d. Die supplier process ID (Mask #):  e. Number of transistors or gates:  f. Number of mask steps: |  | | | |
| 9.2. MEMS Wafer/Die Technology Description:  a. Wafer/Die process technology:  b. Sensor length x width x depth:  c. Sensor anti-stiction coating:  d. Die supplier process ID (Mask #):  e. Number of sensor detection elements (e.g., comb/fingers cells, pressure-sensing cells, thermal cells, etc.):  f. Number of mask steps: |  | | | |
| 9.3. Cap to MEMS Wafer Bonding Technology Description:  a. Bonding process technology:  b. MEMS cavity gas atmosphere after bonding:  c. MEMS cavity pressure range after bonding: |  | | | |
| 10.1. Die Dimensions:  a. Die width:  b. Die length:  c. Die thickness (finished):  d. Membrane Thickness: | Control Die | MEMS Die | | Cap Die |
| 10.2. Capped MEMS Thickness:  a. After bonding:  b. Bonded wafer thinning process description:  c. Finished Capped MEMS die thickness: | Capped MEMS Wafer | | | |
| 11. Die Metallization:  a. Die metallization material(s):  b. Number of layers:  c. Thickness (per layer):  d. % of alloys (if present): | Control Die | MEMS Die | | Cap Die |
| 12. Die Passivation:  a. Number of passivation layers:  b. Die passivation material(s):  c. Thickness(es) & tolerances:  d. MEMS Anti-stiction Coating: | Control Die | MEMS Die | | Cap Die |
| 13.1. Die Overcoat Material (e.g., Polyimide) or Capped MEMS Die (e.g., Gel): | Control Die | | MEMS Die | |
| 14. Die Cross-Section Photo/Drawing: | Control Die  See attached  Not available | MEMS Die  See attached  Not available | | Cap Die  See attached  Not available |
| 15. Die Prep Backside:  a. Die prep method:  b. Die metallization:  c. Thickness(es) & tolerances: | Control Die | MEMS Die | | Cap Die |
| 16. Die Separation Method:  a. Kerf width (μm):  b. Kerf depth (if not 100% saw):  c. Saw method: | Control Die        Single Dual | MEMS Die        Single Dual | | Bonded MEMS Die      Single Dual |
| 17. Die Attach:  a. Die attach material ID:  b. Die attach method:  c. Die placement diagram: | Control Die      See attached  Not available | | MEMS Die      See attached  Not available | |
| 18. Package:  a. Type of package (e.g., plastic, ceramic, unpackaged):  b. Ball/lead count:  c. JEDEC designation (e.g., MS029, MS034, etc.):  d. Lead (Pb) free (< 0.1% homogenous material):  e. Package outline drawing: | Yes  No  See attached  Not available | | | |
| 19.1. Mold Compound:  a. Mold compound supplier & ID:  b. Mold compound type:   1. Flammability rating:   d. Fire Retardant type/composition:  e. Tg (glass transition temperature)(°C):  f. CTE (above & below Tg)(ppm/°C): | UL 94 V1  UL 94 V0      CTE1 (below Tg) =       CTE2 (above Tg) = | | | |
| 19.2. Package Material Used Before or After Mold Over MEMS or Capped MEMS Die:  a. Material type and ID:  b. Minimum material coverage:  c. Maximum material coverage: | Supplier for items b and c shall supply MEMS material coverage drawing with dimensions.          See attached  Not available        See attached  Not available | | | |
| 20.1. Die to Leadframe Wire Bond:  a. Wire bond material:  b. Wire bond diameter (mils):  c. Type of wire bond at die:  d. Type of wire bond at leadframe:  e. Wire bonding diagram: | See attached  Not available | | | |
| 20.2. Die to Die Wire Bond:  a. Wire bond material:  b. Wire bond diameter (mils):  c. Type of wire bond at Control die:  d. Type of wire bond at MEMS die:  e. Wire bonding diagram: | See attached  Not available | | | |
| 21. Leadframe (if applicable):  a. Paddle/flag material:  b. Paddle/flag width (mils):  c. Paddle/flag length (mils):  d. Paddle/flag plating composition:  e. Paddle/flag plating thickness (μinch):  f. Leadframe material:  g. Leadframe bonding plating composition:  h. Leadframe bonding plating thickness (μinch):  i. External lead plating composition:  j. External lead plating thickness (μinch): | Control Die | | MEMS Die | |
| 22. Substrate (if applicable):  a. Substrate material (e.g., FR5, BT, etc.):  b. Substrate thickness (mm):  c. Number of substrate metal layers:  d. Plating composition of ball solderable surface:  e. Panel singulation method:  f. Solder ball composition:  g. Solder ball diameter (mils): |  | | | |
| 23. Unpackaged Die (if not packaged):  a. Under Bump Metallurgy (UBM) composition:  b. Thickness of UBM metal:  c. Bump composition:  d. Bump size: |  | | | |
| 24. Header Material (if applicable): |  | | | |
| 25. Thermal Resistance:  a. JA °C/W (approx):  b. JC °C/W (approx):  c. Special thermal dissipation construction techniques: |  | | | |
| 26. Test circuits, bias levels, & operational conditions imposed during the supplier’s life and environmental tests: | See attached  Not available | | | |

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| 27. Fault Grade Coverage (%) | | | | | % Not digital circuitry | | | | |
| 28. Maximum Process Exposure Conditions:  a. MSL @ rated SnPb temperature:  b. MSL @ rated Pb-free temperature:  c. Maximum dwell time @ maximum process temperature: | | | | | *\* Note: Temperatures are as measured on the center of the plastic package body top surface.*        at       °C (SnPb)        at       °C (Pb-free) | | | | |
| Attachments: | | | | | | | Requirements: | | |
| Die Photo | | | |  | | | 1. A separate Certification of Design, Construction & Qualification must be submitted for each P/N, wafer fab, and assembly location. | | |
| Package Outline Drawing | | | |  | | |
| Die Cross-Section Photo/Drawing | | | |  | | |
| Wire Bonding Diagram | | | |  | | | 2. Design, Construction & Qualification shall be signed by the responsible individual at the supplier who can verify the above information is accurate and complete. Type name and sign below. | | |
| Die Placement Diagram | | | |  | | |  | | |
| MEMS material coverage drawing with dimensions | | | |  | | |  | | |
| Test Circuits, Bias Levels, & Conditions | | | |  | | |
| Completed by: | | Date: |  | | | Certified by: | | Date: |  |
| Typed or Printed: |  | | | | |  | | | |
| Signature: |  | | | | |  | | | |
| Title: |  | | | | |  | | | |