Automotive Electronics Council
Component Technical Committee

ATTACHMENT 11

AEC - Q100-011 Rev-D

CHARGED DEVICE MODEL (CDM)

ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council

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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-011 Rev-D:

- **Section 1.2, Reference Documents: Added ANSI/ESDA/JEDEC JS-002 standard document reference and deleted ESDA S5.3.1 and JEDEC JESD22-C101 standard document references.**
- **Section 2, Additional Requirements (addendum to JS-002): Added new section of specific AEC-Q100-011 requirements beyond those stated in JS-002, including:**
  - **Section 2.1, Tester and Device Preparation**
  - **Section 2.2, Measurements**
  - **Section 2.3, Sample Size**
  - **Section 2.4, Discharge Requirements**
  - **Section 2.5, Detailed Procedure**
  - **Section 2.6, Corner Pin Classification Procedure**
  - **Section 2.7, Small Package Considerations**
  - **Section 2.8, Wafer or Bare Die Considerations**
  - **Section 2.9, Failure Criteria**
  - **Section 2.10, Acceptance Criteria**
  - **Section 2.11, Test Reporting**
- **Table 1, Integrated Circuit CDM ESD Classification Levels: Modified content of Table 1 to align Component Classification and Maximum Withstand Test Condition Levels with JS-002.**
- **Figure 2, Recommended Integrated Circuit CDM ESD Test Flow Diagram: Modified Figure 2 wording to align with JS-002 and newly added Section 2, Additional Requirements (addendum to JS-002).**

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METHOD - 011

CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

All CDM ESD testing performed on Integrated Circuit devices to be AEC Q100 qualified shall be per the latest version of the ANSI/ESDA/JEDEC JS-002 specification with the following clarifications and requirements. Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for integrated circuit devices.

1.2 Reference Documents

ANSI/ESDA/JEDEC JS-002, Charged Device Model (CDM), Device Level

1.3 Terms and Definitions

1.3.1 Corner pins

Pins of an integrated circuit (IC) package that singularly have a higher probability of contact with a grounded surface, based on their package pin geometry. The following leaded package types are expected to have corner pins: Dual in Line (DIP, 4 corner pins), Small Outline Integrated Circuit (SOIC, 4 corner pins), Quad Flat Pack (QFP, 8 corner pins), and Plastic Leaded Chip Carrier (PLCC, 8 corner pins). IC packages for which no pins or balls extend further in the X or Y direction than the package housing, and / or are aligned in an array of equal distribution across a single package surface, may be classified as not having corner pins. Due to the inherent design of the package, QFN (Quad Flat Pack No Lead), WCSP (Wafer Chip Scale Packages) and Ball Grid Arrays (BGAs) with missing pins in the actual corner pin locations do not have corner pins. BGA packages with specific corner pins in the pin array corner are classified as having corner pins (see Figure 1). Engineering judgment shall be made to determine if other packages have corner pins and which pins will be defined as corner pins.

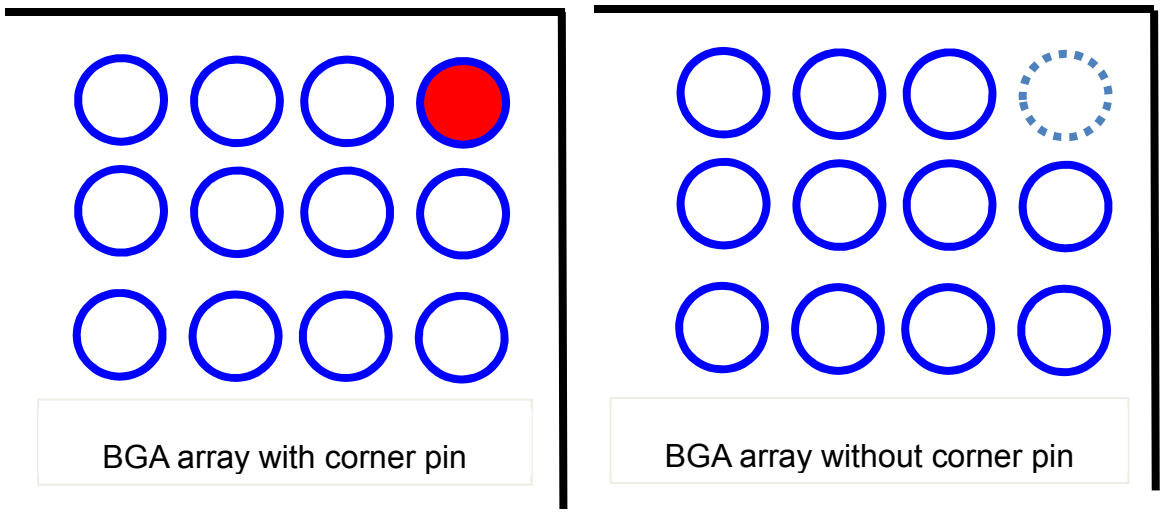


Figure 1: Example BGA package pin arrays with corner pin (left) and without corner pin (right)

2. Additional Requirements (addendum to JS-002)

2.1 Tester and Device Preparation

2.1.1 Devices used for CDM stressing shall not have been used for any prior stress tests.

2.1.2 ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

NOTE: See the latest revision of ANSI/ESD S20.20, JESD625, IEC 61340-5-1 or company-specific handling procedures for guidance.

2.1.3 Devices shall be clean before testing. If needed, cleaning should be completed in compliance with company-approved procedures.

NOTE: Isopropanol (isopropyl alcohol) is typically used for cleaning.

2.1.4 The CDM tester probe and field plate / dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using isopropanol (isopropyl alcohol).

NOTE: Surfaces should be allowed to dry before testing.

2.1.5 Determination and setting of CDM field plate voltage factor and voltage offsets may only be done during full qualification of the CDM test system. Voltage factors and voltage offsets may not be adjusted based on routine waveform verification or based on product test waveforms or results.

NOTE: Section 6.5.2 of JS-002 describes conditions requiring CDM test system qualification or re-qualification.

2.1.6 The same voltage factor adjustments and voltage offsets from qualification shall be used for product at all test conditions and polarities. The qualification procedure described in JS-002 Annex G.1 shall be used for both positive and negative stress determination of offsets to provide separate uniform positive stress offsets and uniform negative stress offsets.

2.2 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.3 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall have all device pins (including power and ground pins) stressed at one (1) test condition stress level. It is permitted to use the same sample group for the next higher test condition stress level if all devices in a sample group meet the acceptance criteria requirements specified in Section 2.10 after exposure to a specified test condition stress level. Test condition level skipping is not allowed. Therefore, the minimum number of devices required for ESD qualification is three (3) devices, while the maximum number of devices depends on the number of stress test condition levels required to achieve the maximum withstanding test condition level. For example, a device with a maximum withstanding test condition level of TC 500 requires 2 stress test condition levels (TC 250 and TC 500) each and 3 devices per test condition level for a maximum total of 6 devices.

Maximum # of devices = (# of test condition levels required) X 3 devices

It is permitted to expand the sample group size per test condition level to allow partitioned pin group stressing, by either polarity and/or pin, as long as every pin is stressed three times positively and three times negatively for three equivalent parts in the expanded sample group, as it would be in the regular sample group. The use of new sample group for each PUT is also acceptable.

2.4 Discharge Requirements

The use of three (3) discharges at each stress level is required. Three (3) positive followed by three (3) negative discharges is also allowed, as well as three alternating sets of positive and negative discharges. Please refer to Annex F of JS-002 for detailed procedure of the single and dual discharge procedures.

2.5 Detailed Procedure

The ESD testing procedure shall be per the recommended test flow diagram of Figure 2 and as follows.

a. Place clean DUT “dead-bug” with device body in direct contact with the dielectric on top of the field plate.

b. Set the tester stress level to + TC 250.

c. Elevate the potential of the DUT by applying the TC 250 voltage to the field plate.

d. Select a PUT and ground (discharge) the DUT, using either discharge method as described in Annex F of JS-002.

e. If using the single discharge procedure, set the tester stress level to negative TC 250, select the same PUT as in step (d) and ground (discharge) the DUT. If using the dual discharge procedure, this step has already been completed.

f. Repeat steps (c) through (e) using the next PUT. The use of a new sample group for each stress polarity is also acceptable.

g. Repeat steps (b) through (f) until every PUT (all device pins, including power and ground pins) is discharged at the specified test condition and polarity.

h. Test the next device in the sample group and repeat steps (a) through (g) until all devices in the sample group have been tested at the specified test condition level and polarity.

i. Submit the devices for complete DC parametric and functional testing (final ATE verification) per applicable device specification and determine whether the devices meet the acceptance criteria specified in Section 2.10. The devices should be ATE tested within 96 hours of ESD testing. Complete DC parametric and functional testing shall be performed at room temperature followed by hot temperature, unless specified otherwise in the device specification. The functionality of "E^2PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each stress test condition level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been stressed.

j. Using the next sample group, increase the stress level by TC 250 and repeat steps (a) through (i). Stress level skipping is not allowed. It is permitted to use the same sample group for the next test condition stress level if all devices in a sample group meet the acceptance criteria specified in Section 2.10 after exposure to a specified test condition stress level. If a device fails at the TC 250 level, decrease the test condition stress level to TC 125 and repeat steps (b) through (i). Use of smaller stress level increments (e.g., TC 50, TC 100, etc.) may be required to determine lower withstand levels.

k. Repeat steps (a) through (j) until failure occurs or the device fails to meet the TC 125 stress test condition.

2.6 Corner Pin Classification Procedure (Table 1, Class C2a)

The class C2a stress procedure may be used if classification testing at the C2 level has passed and classification testing at the C2b level (for all pins) results in failures.

a. To determine the proper CDM classification of corner pins at the C2a level (TC 750), a minimum of three parts shall be stressed using one of the following methods:

Method 1: Stress corner pins only at TC 750
Method 2: Stress all non-corner pins at TC 500, followed by stressing the same three parts for corner pins only at TC 750

b. The C2a stress procedure used shall be reported in the product CDM classification report as either C2a-Method 1 or C2a-Method 2.

c. If all devices in the sample group meet the acceptance criteria specified in Section 2.10, then the device passes the C2a classification level.

2.7 Small Package Considerations

CDM testing of integrated circuits in small packages is very challenging. The vacuum used to hold the package in place during testing is not effective when the package is under a few square millimeters. The capacitance between the device under test and the field plate is also very small, which results in very fast CDM current pulses. These pulses have non-negligible peak currents, but have very fast rise times and very narrow pulse widths, making the pulses impossible to measure with standard 1 GHz measurement systems. Additionally, the total charge within the pulses is so small that CDM failures of integrated circuits in very small packages have seldom been seen. For these reasons, the testing of integrated circuits in very small packages is often not performed (as agreed between supplier and customer) due to the difficulty of testing and the very low chance of failure. Any device or package that could not be completely CDM stressed due to package size shall be recorded.

2.8 Wafer or Bare Die Considerations

The test methods described in this standard may also be used to evaluate components that are shipped as wafers or bare dice. Standardized CDM stressing of wafers or bare dice is not defined due to equipment limitations. Products shipped as bare dice may be placed in a package for purposes of performing CDM stressing, as determined by package test limitations and agreement between supplier and customer. The package used for this stressing shall be recorded.

2.9 Failure Criteria

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification. Complete DC parametric and functional testing immediately following the ESD test provides worst-case data results. For some devices, parametric and functional characteristics may fall outside specified device specification limits when tested immediately after ESD testing, but slowly drift towards acceptable levels over time. If complete DC parametric and functional testing is delayed, the device may be improperly classified at a higher CDM withstand test condition classification level.

2.10 Acceptance Criteria

A device passes a stress test condition level if all devices in the sample group stressed at that test condition level and below pass. All the devices and sample groups used must pass the measurement requirements specified in Section 2.2 and the failure criteria requirements specified in Section 2.9. Using the classification levels specified in Table 1, the supplier shall classify the device according to the maximum withstanding test condition voltage level. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or device package may require reclassification according to this test method.

Table 1: Integrated Circuit CDM ESD Classification Levels

Classification Level	Maximum Withstand Test Condition
C0a	< TC 125
C0b	TC 125 to < TC 250
C1	TC 250 to < TC 500
C2	TC 500 to < TC 750
C2a	TC 500 to < TC 750 (with corner pins [1] ≥ TC 750)
C2b	TC 750 to < TC 1000
C3	TC 1000 [2]

[1] Refer to Section 1.3.1 for description of packages with corner pins. Class C2a level may also be reported by successfully passing the C2 level in a package having no corner pins.

[2] For test conditions above TC 1000, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

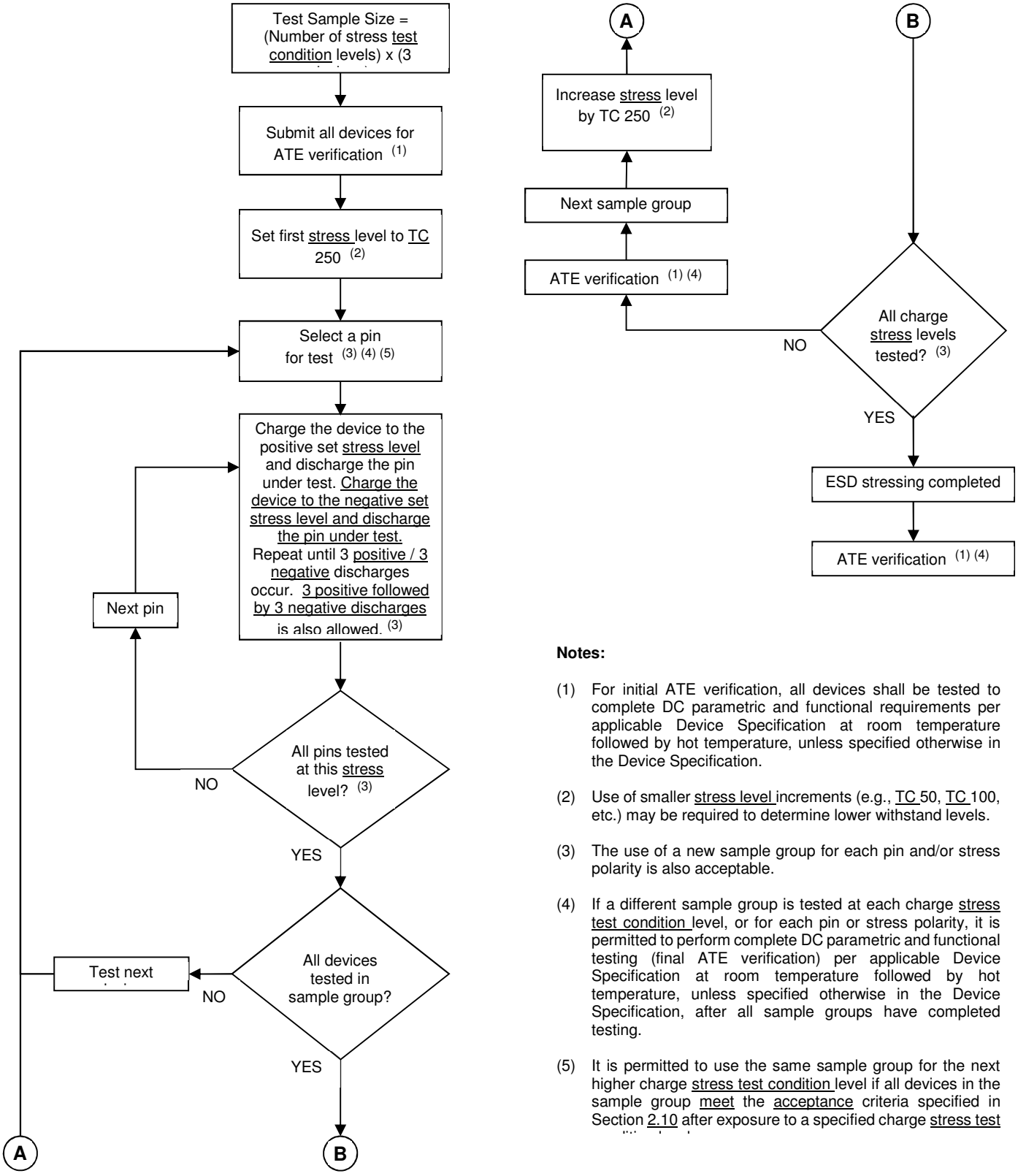
2.11 Test Reporting

Upon completion of the required testing defined herein, a report of the testing performed and detailed results, as defined below, including any deviations, shall be submitted to the user upon request.

a. Sample Details
- Package configuration (e.g., lead pitch, pin count, lead form, etc.)
- Sample sizes

b. Test Details
- Discharging method (e.g., single or dual)
- Stress test condition (TC) levels
- Test/Pin partitioning (if applicable)
- Corner Pin test method (if applicable)
- Package orientation during testing (if simple dead bug orientation cannot be used for a particular package)
- Exceptions to any tests performed
  - Special considerations for small packages
  - Mounting package on a surrogate
  - Wafer/bare die

c. Test Results
- Summary of results



Notes:

(1) For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.

(2) Use of smaller stress level increments (e.g., TC 50, TC 100, etc.) may be required to determine lower withstand levels.

(3) The use of a new sample group for each pin and/or stress polarity is also acceptable.

(4) If a different sample group is tested at each charge stress test condition level, or for each pin or stress polarity, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.

(5) It is permitted to use the same sample group for the next higher charge stress test condition level if all devices in the sample group meet the acceptance criteria specified in Section 2.10 after exposure to a specified charge stress test

Figure 2: Recommended Integrated Circuit CDM ESD Test Flow Diagram

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	Aug. 25, 2000	Initial Release.
A	Jan. 31, 2001	Changed title, revised paragraphs 1.1, 1.2, 3.2, 3.2.1, 3.2.2, revised Table 2 & 3, revised Figure 3.
B	July 18, 2003	Revision to sections 3.6 (j & k) and 5 reflect addition of classification levels for ESD testing and lower voltage step for devices failing 250V. New Table 4 added listing CDM ESD classification levels.
C	July 20, 2012	Complete revision. Revised (and renumbered where appropriate) Acknowledgement and Sections 1.2, 3.1, 3.2, 3.2.3, 3.8 (steps f to j), Table 4, and Figure 5. Added Notice Statement, Sections 1.3.9, 3.6, 3.7, 3.8.1, 6, and new Figure 1. Deleted signature block.
C1	Mar. 12, 2013	Table 4 was revised to correct symbol errors that occurred during the conversion to PDF format. The revision only affects Table 4, Component Classification levels C4B and C6, where the ≥ symbol was inadvertently replaced with the = symbol. No other modifications have been made to the document.
D	Jan. 29, 2019	Complete revision. Added reference to ANSI/ESDA/JEDEC JS-002 as accepted Charged Device Model Standard document. Added new Section 2, Additional Requirements (addendum to JS-002), listing specific AEC Q100-011 conditions beyond those stated in JS-002.